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Patentanmeldung Nr. | Patent application No. | Demande de brevet n°

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Im Auftrag

For the President of the European Patent Office

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R C van Dijk

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Anmelder/Applicant(s)/Demandeur(s):

Koninklijke Philips Electronics N.V.
Groenewoudseweg 1
5621 BA Eindhoven
PAYS-BAS

Bezeichnung der Erfindung/Title of the invention/Titre de l'invention:
(Falls die Bezeichnung der Erfindung nicht angegeben ist, siehe Beschreibung.
If no title is shown please refer to the description.
Si aucun titre n'est indiqué se referer à la description.)

An analog-to-digital conversion arrangement, a signal processing system, and a method for analog-to-digital conversion

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An analog-to-digital conversion arrangement, a signal processing system, and a method for analog-to-digital conversion

The invention relates to an analog-to-digital conversion arrangement for converting an analog input signal into a digital output signal with a most significant part and a least significant part, comprising sample means for sampling the analog input signal, a plurality of course analog-to-digital converters for converting the sampled analog input signal into a course digital signal representing the most significant part of the digital output signal, whereby the course analog-to-digital converters are operated in an interleaved way.

The invention further relates to a system for processing signals.

The invention further relates to a method for converting an analog input signal into a digital output signal with a most significant part and a least significant part, comprising a step sampling the analog input signal by sampling means, a step of converting the sampled analog input signal into a course digital signal representing the most significant part of the digital output signal by a plurality of course analog-to-digital converters operated in an interleaved way.

Such analog-to-digital conversion arrangements are commonly known. A disadvantage of the known analog-to-digital conversion arrangements is that all analog-to-digital converters in the arrangement need to have the accuracy needed to obtain the required resolution of the digital output signal.

Amongst others it is an object of the invention to simplify the design of the analog-to-digital converter arrangement.

To this end the invention provides an analog-to-digital conversion arrangement defined in the opening paragraph which is characterized in that the analog-to-digital conversion arrangement further comprises a fine analog-to-digital converter for converting the sampled analog input signal into a fine digital signal representing the least significant part of the digital output signal, based upon the course digital signal generated by any of said course analog-to-digital converters.

In the analog-to-digital conversion arrangement according to the invention the accuracy of the course analog-to-digital converters may be lower than the accuracy required to obtain the desired resolution of the digital output signal. Only the fine analog-to-digital converter needs to have a high accuracy. In this way the specifications of the course analog-to-digital converters may relaxed, thereby facilitating a simplification of the design of the analog-to-digital conversion arrangement.

The above and other objects and features of the present invention will become more apparent from the following detailed description considered in connection with the accompanying drawings [which disclose an embodiment of the present invention.][in which:]

Fig. 1 shows an embodiment of an analog-to-digital converter according to the invention.

Fig. 1 shows an embodiment of an analog-to-digital converter according to the invention.

For the conversion of each sample a Successive Approximation Analog to Digital Converter needs a number of clock cycles equal to the number of bits that are converted. Also some time must be reserved for the Track and Hold amplifier that precedes the Converter. The settling time in the DAC and the comparator of the SAR ADC determine the maximum clock rate of the conversion process. The maximum sample rate is than determined by the maximum clock rate and the number of clock cycles per sample.

A common method to increase the sample rate is the use of a number of ADC's that are interleaved. These ADC's may share a number of circuit blocks in order to save power and chip area and to prevent or decrease mismatch problems. In this new design four ADC's are interleaved in such a way that they all make use of the same building blocks for the most critical conversion steps. These blocks are the 'Input Buffer', the 'Hold BufferHR', and the '12 bit SAR ADCHR'.

How does it work:

The following example describes 4 interleaving 12 bit converters. The total sequence takes 16 clock cycles so the phase difference between succeeding DACs is 4 clock cycles.

In Phase1 the holdcapacitor C1 is connected to the 'Input Buffer' and the 'Hold Buffer1' So the voltage on C1 is tracking the input voltage and this voltage is buffered to the '8 bit SAR ADC1'.

In Phase 2 and 3 C1 is only connected to 'Hold Buffer1', so in hold condition, and the 8 Most Significant Bits are converted by the '8 bit SAR ADC1'. This converter has a certain kind of overrange capability so the precision, noise and settling accuracy are not critical and power consumption can be low. After this conversion the data are transferred to '12 bit SAR ADCHR' that will do the rest of the conversion.

In Phase4 the holdcapacitor C1 is connected to the 'Hold BufferHR'. It is preferred to precharge the input capacitor of this buffer with the output voltage of 'Hold Buffer1' in order to reduce the effect of charge redistribution of C1 and the input capacitor. The '12 bit SAR ADCHR' than converts the remaining 4 Least Significant Bits and at the end of Phase4 the 12 bit sample is transferred to the output. Of course precision and noise of this converter have to be on a 12 bit level.

System level considerations:

An important quality of AD Converters is low energy consumption. To make a fair comparison between different converters the complete application must be considered. This may include the analog input anti-aliasing filter and the digital output decimation filter depending on the application and the converter principle. It appeared that in the ADC described here the buffers that are used in the Track&Hold circuit are dominant in power consumption even if the interleaving SAR-ADC is oversampled 2 or 4 times compared to the analog bandwidth of the buffers (sufficient low distortion and noise). Active filter sections in front of the buffer (for anti aliasing) consume as much power and add as much noise and distortion as the buffers do. So oversampling is an attractive solution to save power in the anti-aliasing filters and it also prevents folding back of distortion which is a typical problem for Nyquist converters. Practicable values that seem to be feasible for an interleaving SAR-ADC in CMOS18 are an analog bandwidth of 20 MHz and 4 times oversampling at 160 Ms/s at a clock frequency of 640 MHz.

In summary the invention relates to an analog-to-digital conversion arrangement using interleaved analog-to-digital converters, preferably successive approximation analog-to-digital converters. The arrangement according to the invention

results in a very efficient hardware implementation where several circuits are shared by the interleaved converters. In this way offset and gain problems between the converters are decreased. Also hardware complexity is low. A further advantage is that the arrangement according to the invention has a low power consumption.

The embodiments of the present invention described herein are intended to be taken in an illustrative and not a limiting sense. Various modifications may be made to these embodiments by persons skilled in the art without departing from the scope of the present invention as defined in the appended claims.

For instance the method according to the invention may be applied in the processing of other signals than video or audio signals.

CLAIMS:

1. An analog-to-digital conversion arrangement for converting an analog input signal into a digital output signal with a most significant part and a least significant part, comprising

- sample means for sampling the analog input signal,
- a plurality of course analog-to-digital converters for converting the sampled analog input signal into a course digital signal representing the most significant part of the digital output signal, whereby the course analog-to-digital converters are operated in an interleaved way, characterized in that the analog-to-digital conversion arrangement further comprises a fine analog-to-digital converter for converting the sampled analog input signal into a fine digital signal representing the least significant part of the digital output signal, based upon the course digital signal generated by any of said course analog-to-digital converters.

2. An analog-to-digital conversion arrangement as claimed in claim 1, characterized in that course analog-to-digital converters are successive approximation analog-to-digital converters.

3. An analog-to-digital conversion arrangement as claimed in claim 1 or 2, characterized in that the fine analog-to-digital converter is a successive approximation analog-to-digital converter.

4. An analog-to-digital conversion arrangement as claimed in claim 1, 2, or 3, characterized that either the course analog-to-digital converters or the fine analog-to-digital converter are overranging successive approximation analog-to-digital converters.

5. A system for signal processing comprising an analog-to-digital converter arrangement as claimed in claim 1.

6. A system as claimed in claim 4, characterized in that said system is arranged for processing video signals.

7. A system as claimed in claim 4, characterized in that said system is arranged for processing video signals.

8. A method for converting an analog input signal into a digital output signal with a most significant part and a least significant part, comprising

- a step sampling the analog input signal by sampling means
- a step of converting the sampled analog input signal into a course digital signal representing the most significant part of the digital output signal by a plurality of course analog-to-digital converters operated in an interleaved way, characterized in that the method comprises a further step of converting the sampled analog input signal into a fine digital signal representing the least significant part of the digital output signal using the course digital signal generated by any of the course analog-to-digital converters, by a fine analo-to-digital converter.

ABSTRACT:

The invention relates to a method for converting an analog input signal into a digital output signal with a most significant part and a least significant part, comprising a step sampling the analog input signal by sampling means, a step of converting the sampled analog input signal into a course digital signal representing the most significant part of the digital output signal by a plurality of course analog-to-digital converters operated in an interleaved way, the method comprising a further step of converting the sampled analog input signal into a fine digital signal representing the least significant part of the digital output signal using the course digital signal generated by any of the course analog-to-digital converters, by a fine analog-to-digital converter.

Fig. 1

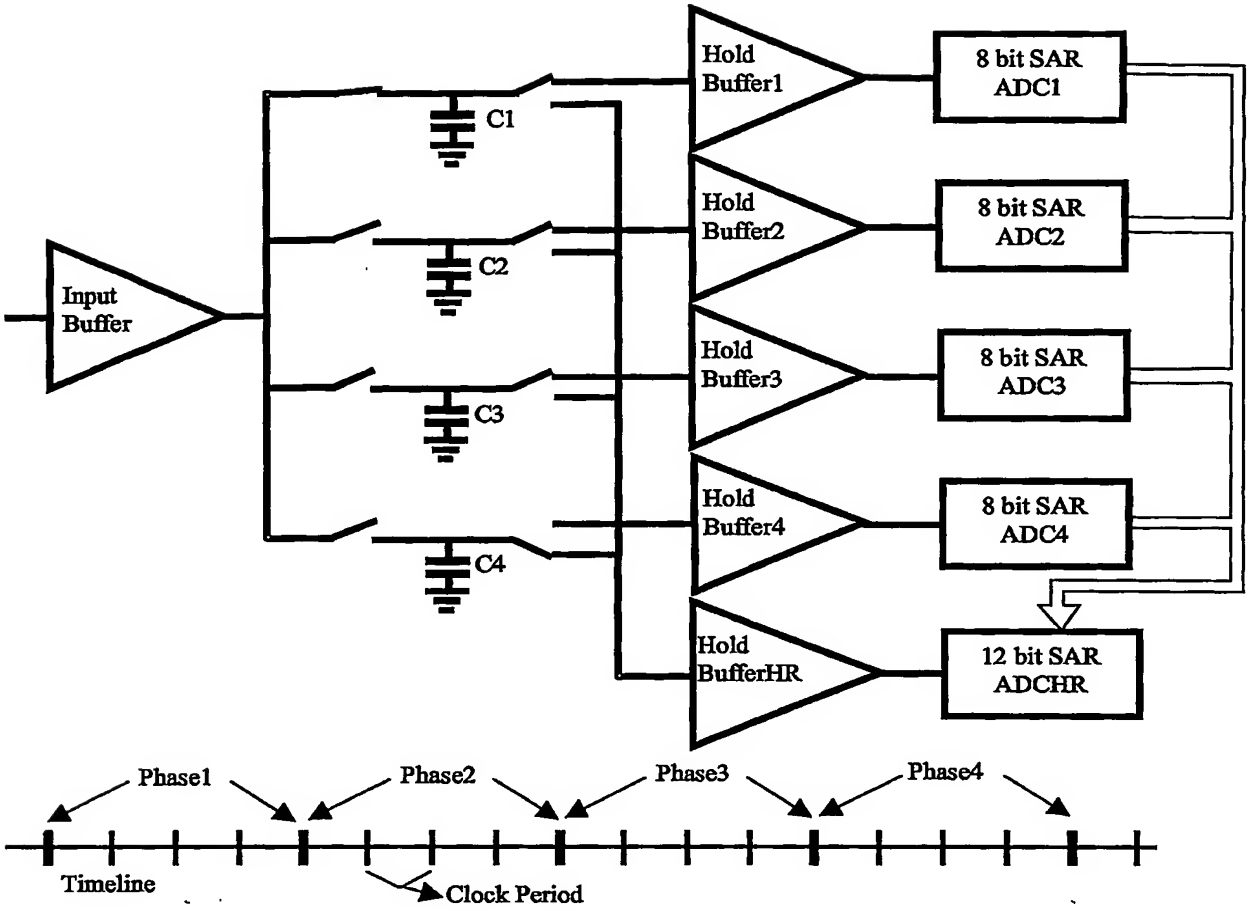
Hold Buffer1
8 bit SAR ADC1
C1
Hold Buffer2
8 bit SAR ADC2
C2
Input Buffer
Hold Buffer3
8 bit SAR ADC3
C3
Hold Buffer4
8 bit SAR ADC4
C4
Hold BufferHR
12 bit SAR ADCHR
Phase1
Phase2
Phase3
Phase4
Timeline
Clock Period

Fig. 1